REMARKS

The Examiner rejected claims 1-20 under 35 U.S.C. §102(b) as allegedly being anticipated by Kruse, James (U.S. Patent 6,530,070).

Applicants respectfully traverse the §102(b) rejections with the following arguments.

35 U.S.C. §102 (b)

The Examiner rejected claims 1-20 under 35 U.S.C. §102(b) as allegedly being anticipated by Kruse, James (U.S. Patent 6,530,070).

Regarding the Examiner's rejections of claims 1 and 9 in bullet #3 of the Office Action, Applicants respectfully contend that Kruse does not anticipate claim 1, because Kruse does not teach each and every feature of claim 1. For example, Kruse does not teach the feature "the first functional block comprises *a mapped location register* residing in one or more FPGA CLBs of the first functional block, and wherein the mapped location register *stores the address* of a current location FPGA element" of claim 1 (italic emphasis added). In Kruse, each element of an RPM (Relationally Placed Macro) in the FPGA can be addressed. This is similar to the case of a memory device (e.g., a Random Access Memory RAM) in which a block of memory cells in the memory device can be individually addressed/accessed. But, Kruse does not disclose a register in the RPM that stores an address of an FPGA element as claimed in claim 1.

Based on the preceding arguments, Applicants respectfully maintain that Kruse does not anticipate claim 1, and that claim 1 is in condition for allowance.

Similarly, Applicants respectfully contend that Kruse does not anticipate claim 9, because Kruse does not teach each and every feature of claim 9. More specifically, Kruse does not teach the feature "providing in the first functional block *a mapped location register* residing in one or more FPGA CLBs of the first functional block; and using the mapped location register to receive and store *the address* of a current location FPGA element" of claim 9 (italic emphasis added). The detailed arguments are similar to those for claim 1 above.

Based on the preceding arguments, Applicants respectfully maintain that Kruse does not

anticipate claim 9, and that claim 9 is in condition for allowance.

Regarding the Examiner's rejections of claims 2 and 10 in bullet #4 of the Office Action, since claim 2 depends from claim 1 which is not anticipated by Kruse as explained above, Applicants contend that claim 2 is likewise not anticipated by Kruse.

In addition, Kruse does not teach the feature "*a mapped destination register* residing in one or more FPGA CLBs of the first functional block, and wherein the mapped destination stores the *address* of a destination FPGA element" of claim 2 (italic emphasis added). In Kruse, each element of a RPM (Relationally Placed Macro) in the FPGA can be addressed. But, Kruse does not disclose a register in the RPM that stores an address of an FPGA element as claimed in claim 2. As a result, claim 2 is not anticipated by Kruse and therefore in condition for allowance.

Similarly, since claim 10 depends from claim 9 which is not anticipated by Kruse as explained above, Applicants contend that claim 10 is likewise not anticipated by Kruse.

In addition, Kruse does not teach the feature "providing further in the first functional block *a mapped destination register* residing in one or more FPGA CLBs of the first functional block; and using the mapped destination register to receive and store the *address* of a destination FPGA element" of claim 10 (italic emphasis added). The detailed arguments are similar to those for claim 2 above. As a result, claim 10 is not anticipated by Kruse.

Regarding the Examiner's rejections of claims 3 and 11 in bullet #5 of the Office Action, since claim 3 depends from claim 2 which is not anticipated by Kruse as explained above, Applicants contend that claim 3 is likewise not anticipated by Kruse.

In addition, Kruse does not teach the feature "*a mapped movement register* residing in

one or more FPGA CLBs of the first functional block, and wherein the mapped movement register *stores the direction and distance of a next step of the movement* of the first functional block" of claim 3 (italic emphasis added). Kruse describes how to address each element of the FPGA, but does not mention forming a register from the elements of the FPGA, let alone using the register to receive and store the "*direction and distance of a next step of the movement* of the first functional block" as claimed in claim 3. As a result, claim 3 is not anticipated by Kruse.

Similarly, since claim 11 depends from claim 10 which is not anticipated by Kruse as explained above, Applicants contend that claim 11 is likewise not anticipated by Kruse.

In addition, Kruse does not teach the feature "providing further in the first functional block *a mapped movement register* residing in one or more FPGA CLBs of the first functional block; and using the mapped movement register to *receive and store the direction and distance of a next step of the movement* of the first functional block" of claim 11 (italic emphasis added). The detailed arguments are similar to those for claim 3 above. As a result, claim 11 is not anticipated by Kruse.

Regarding the Examiner's rejections of claims 4 and 12 in bullet #6 of the Office Action, since claim 4 depends from claim 3 which is not anticipated by Kruse as explained above, Applicants contend that claim 4 is likewise not anticipated by Kruse.

In addition, Kruse does not teach the feature "*a mapped logic location function* configured to *calculate the direction, distance, and time for the next step of the movement* of the first functional block *based on the contents of the mapped location register, the mapped destination register, and a time limit* allowed for the movement of the first functional block" of claim 4 (italic emphasis added). Kruse describes the "RPM" (column 2, line 50) but does not

mention that the RPM is capable of calculating its own direction, distance, and time for its movement as claimed in claim 4, let alone the feature that the movement calculation is based on the contents of some registers and an allowed time limit as claimed in claim 4. As a result, claim 4 is not anticipated by Kruse.

Similarly, since claim 12 depends from claim 11 which is not anticipated by Kruse as explained above, Applicants contend that claim 12 is likewise not anticipated by Kruse.

In addition, Kruse does not teach the feature "providing further in the first functional block *a mapped logic location function*; and using the mapped logic location function to *calculate the direction, distance, and time for the next step of the movement* of the first functional block *based on the contents of the mapped location register, the mapped destination register, and a time limit allowed* for the movement of the first functional block" of claim 12 (italic emphasis added). The detailed arguments are similar to those for claim 4 above. As a result, claim 12 is not anticipated by Kruse.

Regarding the Examiner's rejections of claims 5 and 13 in bullet #7 of the Office Action, since claim 5 depends from claim 1 which is not anticipated by Kruse as explained above, Applicants contend that claim 5 is likewise not anticipated by Kruse. Since claim 13 depends from claim 9 which is not anticipated by Kruse as explained above, Applicants contend that claim 13 is likewise not anticipated by Kruse.

Regarding the Examiner's rejections of claims 6 and 14 in bullet #8 of the Office Action, since claim 6 depends from claim 5 which is not anticipated by Kruse as explained above, Applicants contend that claim 6 is likewise not anticipated by Kruse.

In addition, Kruse does not teach the feature "the first functional block is *configured to*

move to the second localized IO circuit *within a time limit*" of claim 6 (italic emphasis added). Kruse does not teach moving the RPM within a time limit as claimed in claim 6. As a result, claim 6 is not anticipated by Kruse.

Similarly, since claim 14 depends from claim 13 which is not anticipated by Kruse as explained above, Applicants contend that claim 14 is likewise not anticipated by Kruse.

In addition, Kruse does not teach the feature "*moving* the first functional block to the second localized IO circuit *within a time limit*" of claim 6 (italic emphasis added). Kruse does not teach moving the RPM within a time limit as claimed in claim 14. As a result, claim 14 is not anticipated by Kruse.

Regarding the Examiner's rejections of claims 7 and 15 in bullet #9 of the Office Action, since claim 7 depends from claim 5 which is not anticipated by Kruse as explained above, Applicants contend that claim 7 is likewise not anticipated by Kruse. Since claim 15 depends from claim 13 which is not anticipated by Kruse as explained above, Applicants contend that claim 15 is likewise not anticipated by Kruse.

Regarding the Examiner's rejections of claims 8 and 16 in bullet #10 of the Office Action, since claim 8 depends from claim 1 which is not anticipated by Kruse as explained above, Applicants contend that claim 8 is likewise not anticipated by Kruse.

In addition, Kruse does not teach the feature "*connections* electrically coupling each FPGA element to surrounding FPGA elements such that the *contents of all FPGA elements in a functional block can be transferred to their non-adjacent FPGA elements in one clock cycle*" of claim 8 (italic emphasis added). Kruse does not teach any connections in the FPGA that allows

transfer of contents of the elements of the RPM to non-adjacent FPGA elements in one clock cycle as claimed in claim 6. As a result, claim 6 is not anticipated by Kruse.

Similarly, since claim 16 depends from claim 9 which is not anticipated by Kruse as explained above, Applicants contend that claim 16 is likewise not anticipated by Kruse.

In addition, Kruse does not teach the feature "*providing connections* electrically coupling each FPGA element to surrounding FPGA elements such that the *contents of all FPGA elements in a functional block can be transferred to their non-adjacent FPGA elements in one clock cycle*" of claim 6 (italic emphasis added). Kruse does not teach providing any connections in the FPGA that allows transfer of contents of the elements of the RPM to non-adjacent FPGA elements in one clock cycle as claimed in claim 16. As a result, claim 16 is not anticipated by Kruse.

Regarding the Examiner's rejection of claim 17 in bullet #11 of the Office Action, Applicants respectfully contend that Kruse does not anticipate claim 17, because Kruse does not teach each and every feature of claim 17. For example, Kruse does not teach the feature "forming *a mapped location register* residing in one or more FPGA CLBs of the first functional block; loading the mapped location register with *an address of a current location FPGA element*" of claim 17 (italic emphasis added). In Kruse, each element of an RPM (Relationally Placed Macro) in the FPGA can be addressed. This is similar to the case of a memory device (e.g., a Random Access Memory RAM) in which a block of memory cells in the memory device can be individually addressed/accessed. But, Kruse does not describe forming any register in the RPM let alone loading the register with an address of an FPGA element as claimed in claim 17. As a result, Kruse does not anticipate claim 17.

Regarding the Examiner's rejection of claim 18 in bullet #12 of the Office Action, since

claim 18 depends from claim 17 which is not anticipated by Kruse as explained above, Applicants contend that claim 18 is likewise not anticipated by Kruse.

In addition, Kruse does not teach "*assigning all the FPGA elements* of the first functional block *a unique function number*" of claim 18. In other words, all the *FPGA elements* of the first functional block are assigned the same unique function number. In contrast, the reference numeral 301 in Kruse is used to refer to the entire functional block 301 (FIGs. 3A and 3B of Kruse). In Kruse, each element of the FPGA does not have a unique function number. Even if the assigned address of an element of the FPGA is considered its assigned function number, the function numbers of the elements of the RPM are not the same as claimed in claim 18. As a result, claim 18 is not anticipated by Kruse.

Regarding the Examiner's rejection of claim 19 in bullet #13 of the Office Action, since claim 19 depends from claim 17 which is not anticipated by Kruse as explained above, Applicants contend that claim 19 is likewise not anticipated by Kruse.

In addition, Kruse does not teach "*forming a mapped destination register* residing in one or more FPGA CLBs of the first functional block; *loading the mapped destination register with the address* of a destination FPGA element" of claim 19 (italic emphasis added). The detailed arguments are similar to those for claim 10 above. As a result, claim 19 is not anticipated by Kruse.

Regarding the Examiner's rejection of claim 20 in bullet #14 of the Office Action, since claim 20 depends from claim 19 which is not anticipated by Kruse as explained above, Applicants contend that claim 20 is likewise not anticipated by Kruse.

In addition, Kruse does not teach "*forming a mapped logic location function* in the first

functional block; and using the mapped logic location function to *calculate the direction, distance, and time for the next step of the movement* of the first functional block *based on the contents of the mapped location register, the mapped destination register, and the time limit allowed*" of claim 20 (italic emphasis added). The detailed arguments are similar to those for claim 12 above. As a result, claim 20 is not anticipated by Kruse.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Date: August 17, 2005

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